

Designing for Compliance 1999

Part 2

Rethinking the Role of Power and Return Planes

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Conventional wisdom has it that good EMC practice requires closely spaced power and return planes. Our most recent experiments, however, indicate there may be a better use for PCB planes than just to distribute power, namely to provide shielding.

We'll start right in with an experiment.

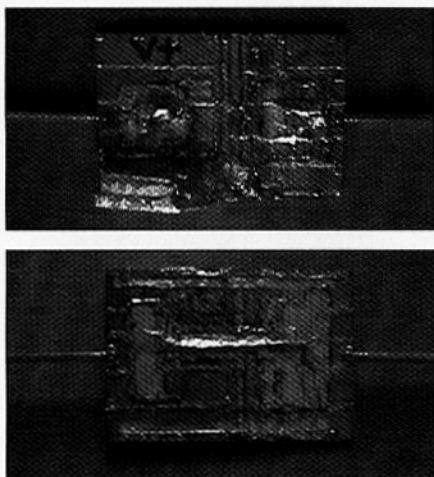
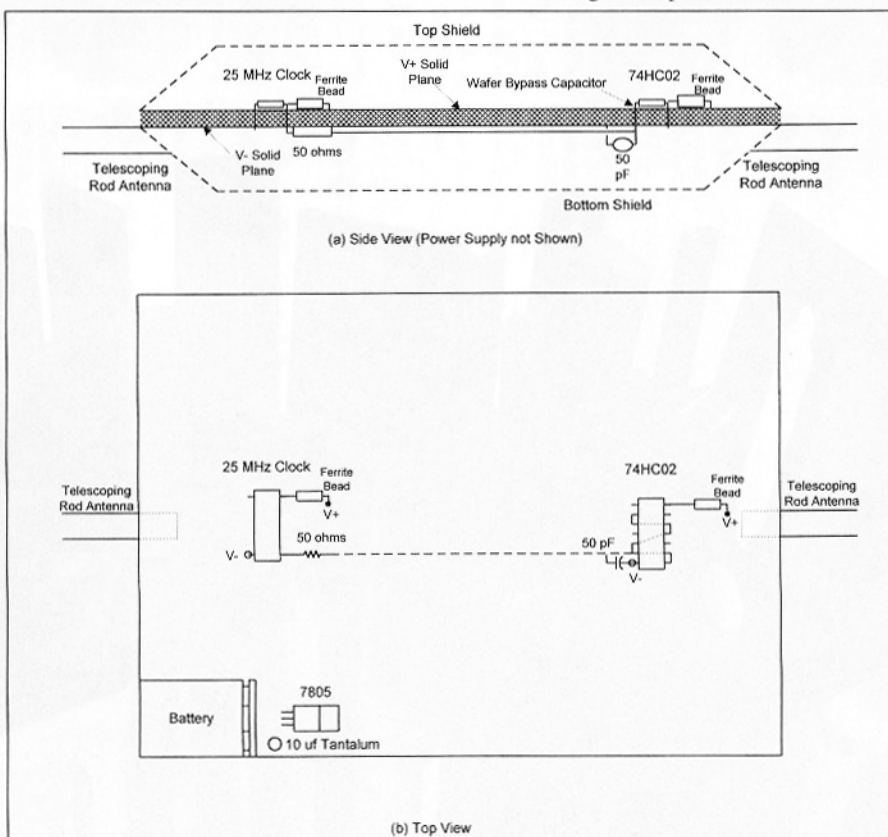
The circuit that we will use is the circuit shown in Figure 1 (a) and (b) and is basically the circuit that we have been analyzing in this series of articles for more than a year. A clock driver, running at 25 MHz using HC technology drives an HC load. Techniques commonly thought of as good EMC practice are used throughout: beneath each IC is placed a wafer type low inductance capacitor, the run connecting the clock driver to its load is straight and placed immediately adjacent to the return plane and a damping resistor is in use.

Telescoping antenna elements are connected to the return plane and extended out 19 inches from either edge of the board, simulating the use of I/O cables (which can be considered directly or incrementally connected to the return in most designs.) Our telescoping elements experimentally produce a system resonance at 125 MHz, the 5th harmonic of the clock.

Despite its simplicity, the circuit produces significant radiation. In past arti-

cles, we have explored the reasons for this (Figure 2). Even a solid return plane has a finite inductance which causes a voltage drop across its length. That voltage drop drives any connected I/O cables (telescoping antenna elements in our set up) to radiate as if they were antennas. The amount of radiation we had detected matched reasonably well that predicted by theory. [1]

In producing this current set of results, we took things a little further. We covered both the top and the bottom of our circuit with copper foil, producing what were, in effect, shields on the top and bottom of the board. Everything was covered, the batteries, the ICs and the connections between the clock driver and its distant load. The device under test (DUT) is shown in Figures 1(c) and (d). Where seams of the copper tape came together, solder was used to ensure a good electrical connection which accounts for the rough appearance. Note, however, that the device of Figure 1 is not using a complete shield. The



Figures 1C and 1D.

Figure 1. The device we tested first had shields over the top and bottom of the PCB, the top shield connected to V+ and the bottom to V-. The "shields" were formed with copper tape, soldered at the seams.

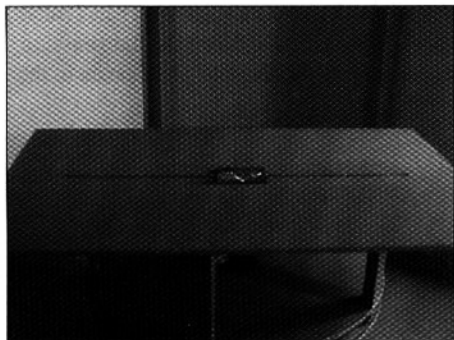


Figure 2. The test setup. Note the telescoping elements used to simulate I/O cables.

top shield is still separated from the bottom shield, the top shield being connected to V+ and the bottom shield, V-. Still, shielding is complete except for the gap between V+ and V- represented by the dielectric between the PC board's two planes.

Emission results are shown in Figure 5 and are unimpressive. The circuit radiates quite strongly. This seems to illustrate at least two things: First, completely shielding the two halves of our printed circuit board does not a complete shield produce. The DUT continues to radiate, prominently at some frequencies. Second, it illustrates that EMC can be a frustrating profession. We have managed to cover the top and bottom of the boards with enough copper tape to have reached from our test stand to our antenna and back, but to little avail.

Why would such a device radiate so much energy? We believe the answer lies in the following analysis. The source of the emissions arises from a phenomenon we have noted in our earlier articles [2]. When MOS technology switches, there is a moment in time in the transition when both the P and N channel FETs are on at the same time. A brief burst of noise known as Idd Delta, or simply Idd Noise, is produced. For most MOS technologies, the pulse is very narrow, on the order of hundreds of picoseconds to a few nanoseconds, and on the order of 1-10 milliamps in amplitude. Such impulsive noise pro-

duces significant energy at frequencies well up the spectrum from the fundamental. This energy passes onto the power planes which can be thought of as a kind of parallel plate transmission line. The impedance of a parallel plate transmission line is well known.

$$Z_o \approx \frac{377}{\sqrt{\epsilon_r}} \left(\frac{d}{w} \right) = \sqrt{\frac{\mu_o}{\epsilon_r \epsilon_o}} \left(\frac{d}{w} \right) \quad (1)$$

Where:

d = distance between the planes in meters

w = width of the planes in meters

ϵ_r = relative permittivity

ϵ_o = dielectric constant = 8.85×10^{-12}

The impedance of any transmission line is a function of its lumped capacitance and inductance. As for the capacitance that too is well known:

$$C = \frac{w \epsilon_r \epsilon_o}{d} \quad (2)$$

Where:

C = capacitance in farads per unit length (meters)

That allows us to calculate the inductance per unit length.

$$Z = \sqrt{\frac{L}{C}} \quad (3, 4)$$

$$L \approx Z^2 C = \frac{\mu_o}{\epsilon_r \epsilon_o} \frac{d^2}{w^2} \frac{w}{d} \epsilon_r \epsilon_o = \mu_o \frac{d}{w}$$

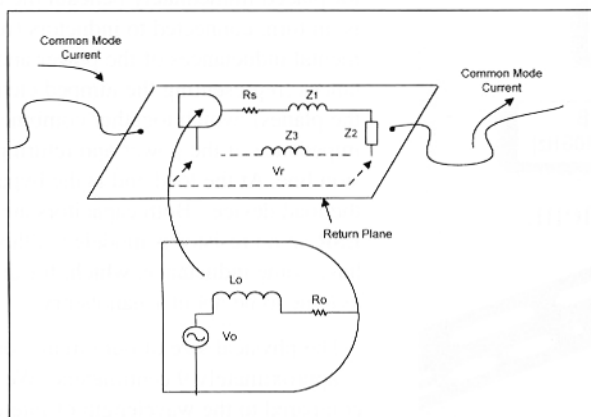


Figure 3. As our previous articles have discussed, radiation is caused when currents pass through the finite impedance of the return plane (Z_3), producing a voltage drop (V_r) which causes attached cables to radiate. The clock is modeled as a voltage source with an internal inductance and resistance. The signal trace is modeled as an inductor (Z_1) and the driven gate as an undefined load impedance (Z_2).

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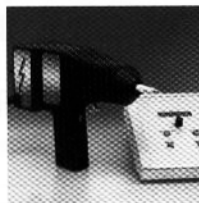
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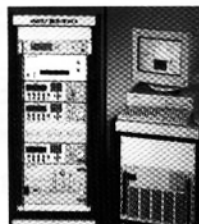
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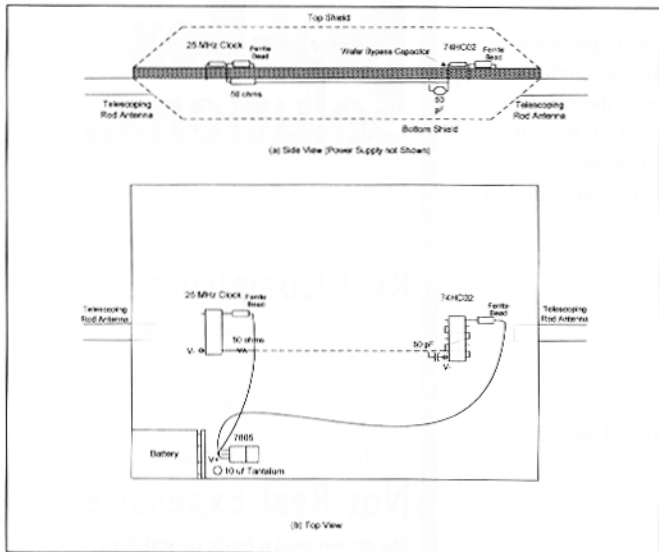


Figure 4. Defying convention, we sought to lower emissions by hard wiring the IC's to the supply with ordinary wires, isolating the top shield from V+ and then connecting both shields together. Emissions dropped significantly

Where:

L = Inductance per unit length (meters) in Henries

μ_o = free space permeability = $4\pi \times 10^{-7}$

It is the inductance that gives rise to our problems, specifically the partial inductance of the return plane. Since the transmission line is symmetrical, we can assign half the total inductance to the return meaning that its inductance is:

$$L_{return\ plane} \approx \frac{\mu_o}{2} \left(\frac{d}{w}\right) \frac{Henries}{meter} \quad (5)$$

For our device, d=1.6mm and w=11.5cm, resulting in a return inductance of approximately .09 nH/cm.

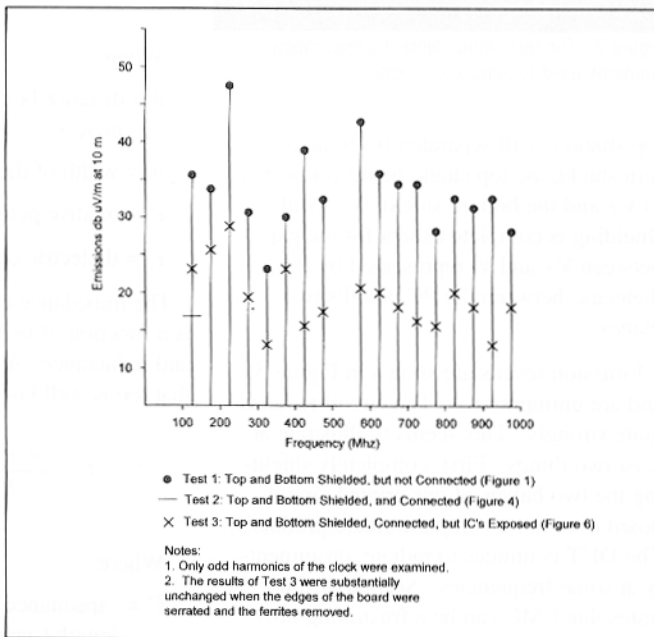


Figure 5. Our comparative emissions results.

Having derived the inductance of the return plane we can draw a circuit to describe the phenomenon we are observing (Figure 7(a)). Here a current source, which we define as impulsive with fundamental frequency of 25 MHz and of an amplitude of 1-10 milliamps, drives a nearby capacitor, which is the bypass capacitor placed immediately beneath the clock driver. That capacitor is, in turn, connected to inductors (representing the lumped elemental inductances of the power and return planes) and capacitances (representing the lumped elemental capacitances between the planes), which together combine to produce the characteristic impedance of the power and return planes modeled as a transmission line. At the load end is the bypass capacitor placed across the load device. Both capacitors are assumed to have very low ESR so no resistor is modeled, although they are assumed to have some inductance, which, for the purpose of our analysis, we assume to be about 1 nanohenry.

The physical size of our circuit connecting the clock to the load is approximately 9 centimeters. We know if the circuit is small compared to the wavelength of interest (less than 1/10th of a wavelength) then we can ignore transmission line effects which eases our analysis. Therefore, for the first few harmonics of the clock, we can analyze the circuit using the simplified model shown in Figure 7(b). Here, we have assumed that we are operating at a frequency above the resonant frequency of the bypass

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board itself becomes a transmission line terminated, here and there with bypass capacitances and other devices, and, at its edges, not at all. Clearly the notion that closely placed power and ground planes serves as a simple capacitor and, thereby a low impedance which essentially shorts out I_{dd} Noise, is entirely too simplistic. Rather, significant emissions can still result from the "well shielded" circuit of Figure 1 owing to at least three factors, (1) the partial impedance of the return plane, (2) resonances caused by the combination of various inductances and capacitances, and (3) at higher frequency, transmission line effects from the power planes acting as a poorly terminated transmission line.

Some authors have attempted to control emissions by flattening the impedance presented by power planes by avoiding resonances [3]. We propose a different approach, the use of planes to provide shielding rather than merely lowering the power supply impedance.

Figure 4 doesn't look very much different than Figure 1, but there is a crucial distinction. Here the top and bottom shields are connected together and the top shield isolated from the supply. Internally, we've routed wires from our power supply to pin 14 of both ICs. This time when emissions are measured, the fall is dramatic (Figure 5). Only one emission is found at all greater than 5 uV/m at 10m, it being at 125 MHz and about 20 dB down from the device of Figure 1.

The reason for the dramatic fall is quite simple, we now have a Faraday cage and it is working the way that we would expect.

Figure 4 simply confirms what we already know, that if you put a nearly complete shield around a circuit, it doesn't radiate very much. However, that is often not really much of a practical option. In order to test a more practical solution, we remove the shielding over the integrated circuits as shown in Figure 6. While radiation did increase, the reduction in emissions as

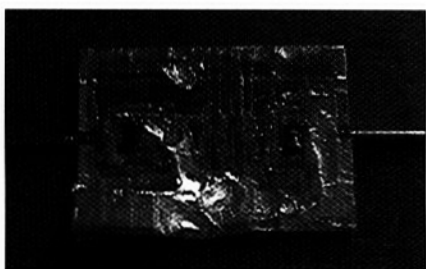


Figure 6. We modified the device of Figure 4 by removing the shields over the IC's. Emissions rose, but were still significantly lower than those detected from the device illustrated in Figure 1.

capacitors, but below the frequencies at which the power and ground planes act as a transmission line.

In this range of frequencies, we can readily observe why our shields did not work. Something close to one half of our I_{dd} Noise ended up flowing along the surface of our bottom shield which exhibits a small but still significant inductance. The voltage V_r dropped across the return shield's impedance caused the attached telescopic antennas to radiate like a dipole.

Real world circuits are, of course, quite a bit more complicated. Add more bypass capacitors and more sources, and predicting V_r can become quite a complicated task. At higher frequencies the

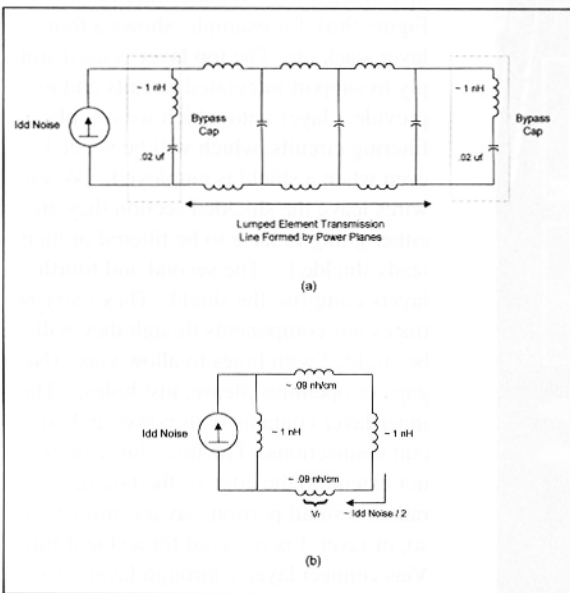


Figure 7. Even "solid" supply planes are difficult to accurately model. Bypass capacitors and the transmission line characteristics of the planes themselves must be considered. By limiting the frequencies of interest, the model can be simplified as in (b).

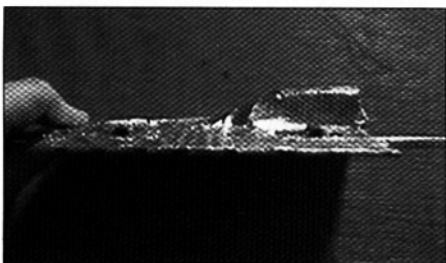


Figure 8. We serrated the edge of the fully shielded device of Figure 4. Emissions were not noticeably affected.

compared to the basic circuit of Figure 1 was still dramatic.

We are not contending that providing a low impedance power source to integrate circuits is not important — it is. However, it is not key, necessarily, to reducing emissions. Providing a low impedance power source will improve noise margin. Such a power distribution system, however, should be designed to be both low impedance and relatively free

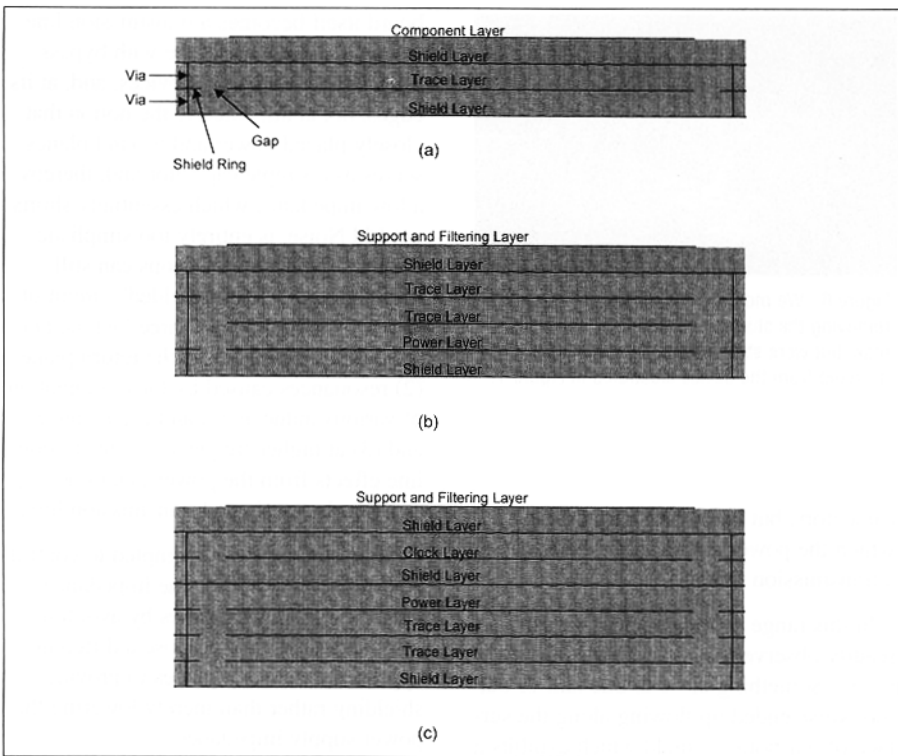


Figure 9. Some suggested (but as yet untested) stack ups.

of resonances. Simply providing a nearly complete power and ground plane (complete in the sense that it lacks gaps) may not necessarily do the job because of effects noted above.

In Figure 9 we have illustrated some possible (but as yet untested) PCB stack ups which should reduce emissions. Figure 9(a), for example, shows a four layer stack up. The top layer is used simply to support integrated circuits and to provide a layer onto which we can place filtering circuits, which will be needed even when a shield is employed. (When wires leave the shielded section they are either going to have to be filtered or their leads shielded.) The second and fourth layers comprise the shield. They carry no traces nor components though they will be studded with holes to allow vias. (No gaps or openings please, just holes.) The inner layer contains both power and circuit connections. The inner layer does not extend to the edge of the board, rather, a small portion, say a centimeter or so, of layer 3 is reserved for a shield ring. Vias connect layer 2 through layer 3 to layer 4. Only extremely simple boards can use this stacking, because only one layer is available for traces.

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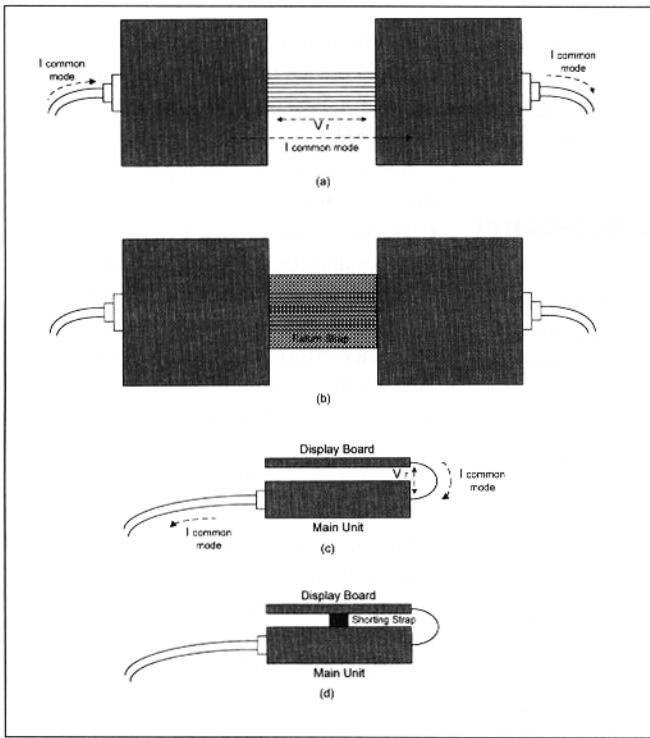


Figure 10. Even two well shield PCBs may radiate if interconnected with multiconductor cable carrying high frequency currents. The impedance of these wires causes a voltage drop that drives the two PCBs and their attached shielded cables as if they were two halves of a dipole. A return strap can be used to "short out" V_r as shown in (b). Other designs can exhibit similar problems, but similar solutions can be employed as illustrated in (c) and (d).

The four layer stack up of Figure 9(a) doesn't allow for much circuitry or for a power distribution network, so the six layer stack of Figure 9(b) could find application in more practical circuits. Again, the top layer is used for support and filtering, layers 2 through 6 comprise the shield. The outer centimeter or so of layers 3, 4 and 5 are reserved for the shield rings around each layer and these connect to the vias which connect layers 2 through 6 together at their edges, comprising the shield.

Naturally, the circuit and power layers could be reversed if desired.

An 8 layer stack up is shown in Figure 9(c).

There are as many variations on this theme as there are combinations of circuit, power and shield layers, but all share a common theme. All of the circuitry, including power distribution, is trapped within a shield consisting of two of the outer layers on the board connected together through the use of vias and shield rings on the intervening layers. Wires that exit the shield will radiate unless they are somehow treated by either bypassing, some other form of filtering (ferrites), a combination of the two, or by the use of a shielded cable.

Finally, among the most challenging configurations are those involving two or more boards. One possible set up is shown in Figure 10. Both boards have been designed to take advantage of the concepts which we have described in this article, that is, outer layers have been reserved for support and shielding. The problem is that the connection between the two boards consists of many wires in a geometry that makes both filtering and shielding

impractical. One way around this dilemma is to provide a shorting strap as shown in Figure 10(b). While the connection between the two boards is inductive and would produce a voltage drop between the two boards and cause them and the attached cables to radiate as if they were antennas, the shorting strap essentially shorts out this voltage and greatly lessens the accompanying radiation.

The same phenomenon has been observed when high speed signals run through a ribbon cable which connects a peripheral board, such as a display board, with a mother board (Figure 10(c)). Here the cable attached to the mother board may radiate significantly, even if the mother board is shielded and a shielded cable is attached to it. The inductance of the ribbon cable causes a voltage drop between the display board and the mother board. This in turn causes the mother board and its attached cable to act as one side of a rather lopsided antenna system and the display board as its counterpoise. One solution is to short out the voltage source, V_r , with a short, fat shorting bar or strap as shown. ■

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