SAMPLE FORMAL REPORT

MEASUREMENT OF

COMMON MODE REJECTION RATIO

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ABSTRACT

A technique for measuring the common mode rejection ratio of an operational amplifier is described. The theoretical basis for the measurement is developed, and the corresponding laboratory procedure is discussed. Results of some actual measurements with a 741 operational amplifier are provided.

BASIS FOR COMMON-MODE REJECTION MEASUREMENTS

The circuit that was used for the common mode rejection ratio (CMRR) measurement is shown in Fig. 1 (page 7). In order to eliminate errors resulting from bias and offset parameters, the measurement should be performed at ac rather than dc. However, since CMRR typically displays a decrease as the frequency is increased beyond some reasonably low frequency reference, the actual measurement frequency must be carefully selected.

The equivalent circuit leading to the measurement concept is shown in Fig. 2 (page 7). Observe that the effect of CMRR is represented by a fictitious generator placed in the non-inverting input. The output voltage V_o is obtained by the procedure that follows..

Assume that the differential input voltage is forced to be zero by feedback. The voltage V^- at the inverting input terminal is the same as voltage at the non-inverting terminal and is

$$V^- = V_i + \frac{V_i}{CMRR} \qquad \textbf{(1)}$$

The current I_i is

$$I_i = \frac{V^- - V_i}{R_1} \qquad \textbf{(2)}$$

Substitution of (1) in (2) leads to

$$I_i = \frac{V_i}{R_1(CMRR)} \qquad \textbf{(3)}$$

The output voltage V_o is

$$V_o = V^- + R_2 I_1 \quad \textbf{(4)}$$

Substitution of (1) and (3) in (4) yields

$$V_o = V_i + \frac{V_i}{(CMRR)} + \frac{R_2 V_i}{R_1 (CMRR)} = V_i + \frac{V_i}{(CMRR)}\left(1 + \frac{R_2}{R_1}\right) \quad \textbf{(5)}$$

Solving for CMRR in (5), the result is

$$CMRR = \frac{V_i}{V_o - V_i}\left(1 + \frac{R_2}{R_1}\right) \quad \textbf{(6)}$$

The result of equation (6) indicates that to determine CMRR, V_i and V_o (or V_i and V_o - V_i) are first measured. Assuming R_2 and R_1 are both known, CMRR is determined from (6).

DESIGN OF MEASUREMENT CIRCUIT

Some care must be exercised in designing a measuring circuit due to the sensitivity of the measurement. For a typical value of CMRR of 10^4 or more and a moderate value of closed-loop voltage gain of $A_{CL} = 1 + R_2 / R_1$, the difference V_o - V_i from equation (5) will be very small and difficult to measure. To enhance the measurement, A_{CL} can be increased. However, the closed loop 3 dB bandwidth is $B_{CL} = B/A_{CL}$, where B is the unity gain frequency. As the 3 dB bandwidth is decreased,

the frequency range over which an accurate measurement can be made decreases. The measurement is also enhanced for larger values of output voltage, but the slew rate limitations may then be more troublesome. Thus, the design of the measurement circuit involves a tradeoff between the possible accuracy in the measurement of $V_o - V_i$ and the frequency range for which CMRR can be established.

Since no particular upper frequency range was specified, a reasonable design compromise was established with R_1 = 100O and R_7 = 10 kO. This results in $A_{CL} = 1 + R_2/R_1 = 101$. For a 741 operational amplifier with B = 1 MHz, the 3 dB bandwidth is 1 MHz/101 = 9.9 kHz. For an assumed output voltage of 9 V and S = 0.5 V/µs, the slew rate limiting frequency is $f_{SR} = 0.5 \times 10^6/(2 \times 9) = 8.84$ kHz. The measurement should be reasonably valid to a frequency somewhat lower than these values.

No attempt was made to plan a measurement of CMRR at dc. Such a measurement requires very special care due to the presence of the input offset voltage and the bias currents, which are of the same order of magnitude as the common mode components. However, by measuring CMRR at ac only, the effects of offset and bias components are eliminated.

MEASUREMENT OF COMMON-MODE REJECTION RATIO

The circuit of Fig. 1 was connected with R1 = 100O, R_2 = 10 kO and a 741 operational amplifier. The input sinusoidal signal voltage was established at 9 V RMS, and this value was maintained in all the measurements. This voltage corresponds to a

peak value of $\sqrt{2} \times 9 = 12.728\ \text{V}$. This voltage is sufficiently lower than the magnitudes of the ±15 V supplies to ensure operation below the saturation region, and this point was carefully checked with the oscilloscope.

At each frequency, the voltage was checked to ensure that it remained constant. Because v_i and v_o are so close, particularly at low frequencies, significant error could have occurred if they had been measured separately and the difference taken. Instead, the net voltage $v_o = v_i$ was measured directly between the output and the input terminals. This measurement was possible because the voltmeter used has a "floating" input. Such a measurement is not possible with a voltmeter having a common ground lead.[1]

Following the measurement of v_i and $v_o - v_i$, CMRR was calculated at each frequency with equation (6). The corresponding decibel measurement CMRR (dB) was then calculated as

$$CMRR(dB) = 20\log_{10} CMRR \qquad \textbf{(7)}$$

The results of the CMRR measurements are summarized in Table 1 (page 9). These data are displayed graphically in Fig. 3 (page 8). A smooth curve has been extrapolated between measured points. In view of the constant level between 25 and 50 Hz, it is expected that the dc value for CMRR (dB) is about 82 dB. This compares favorably with the published range of 70 to 90 dB for a 741 as given in manuals.[2] The rolloff characteristic also is typical of published data up to about 1 kHz or so. However, the apparent "rise" above the 6 dB/octave rolloff rate above 1 kHz is believed to

represent an error. This error arises from the finite 3 dB bandwidth of the closed-loop measurement circuit. The gain is down 3 dB just below 10 kHz, and this causes CMRR to appear larger than the actual value.

SUMMARY AND CONCLUSIONS

A method for measuring the common mode rejection ratio of an operational amplifier has been investigated. The theoretical basis for the measurement has been analyzed, and actual laboratory measurements have been performed. Results obtained compare favorably with published data for the common mode rejection ratio.

Limitations of the measurement procedure have been noted and discussed. Specifically, there is a tradeoff between the frequency range over which the measurement can be performed and the necessity to measure very small voltages accurately. As the frequency range of the circuit is increased, more delicate means must be used for measuring the resulting small voltages in the circuit. This limitation could be partially circumvented by redesigning the measurement circuit to have a lower gain as the frequency is increased.

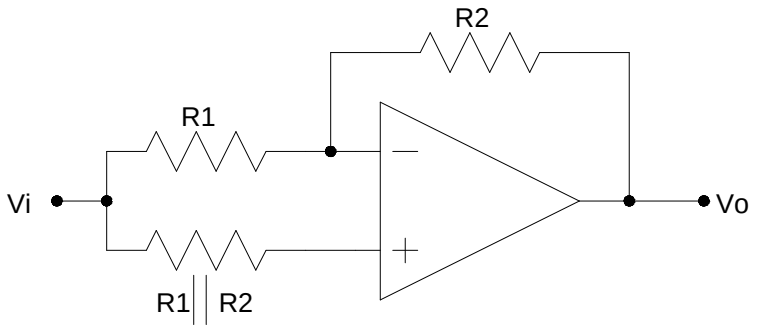

Figure 1 - Circuit used in measuring CMRR.[3]

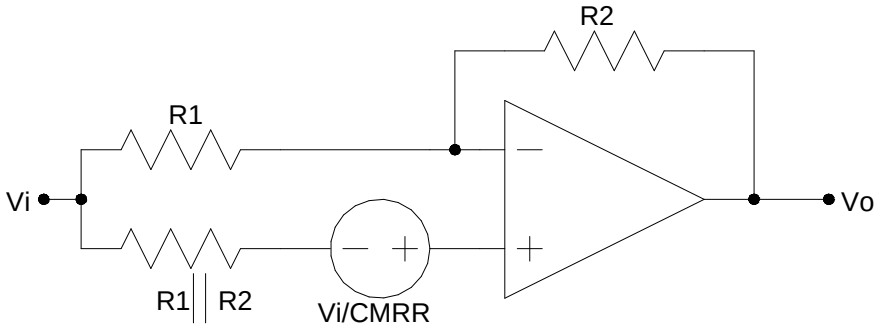

Figure 2 - Equivalent circuit used to analyze CMRR measurement technique.[4]

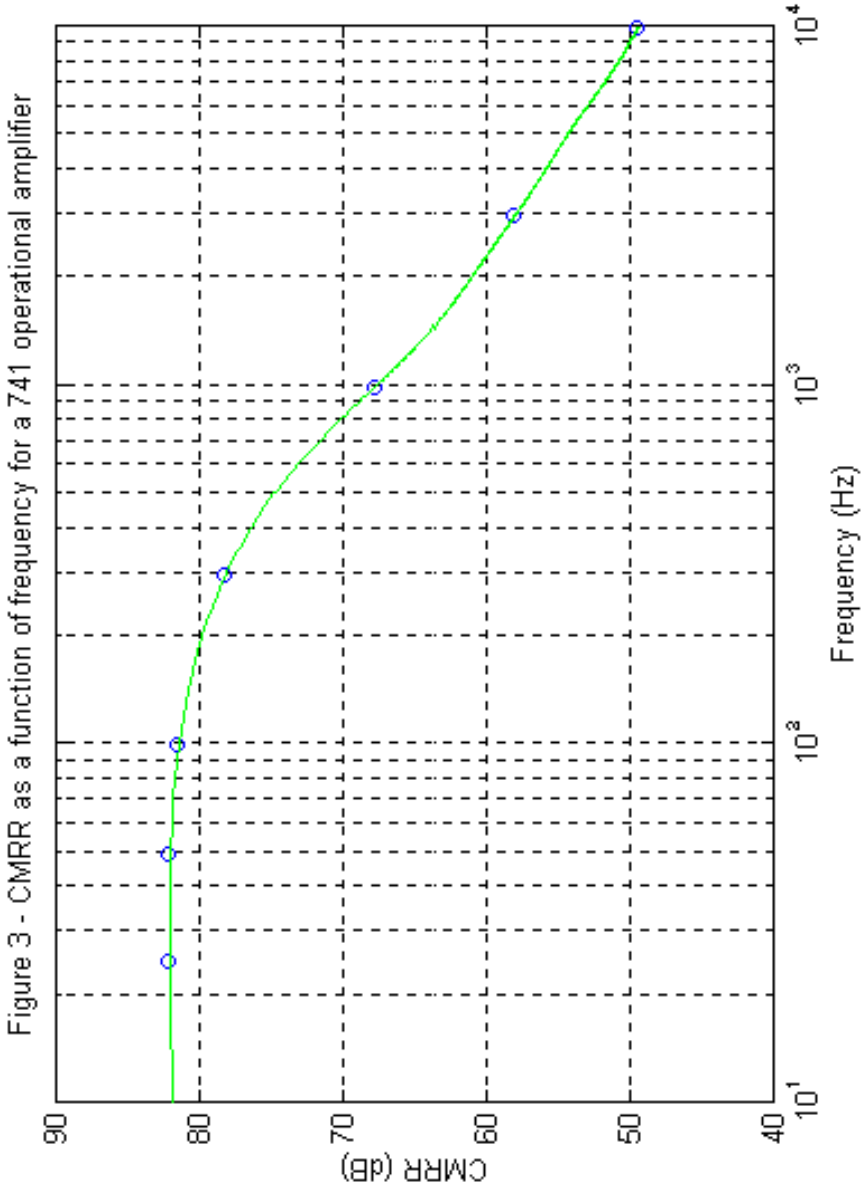

Figure 3 - 741 Op Amp Device Graph.[5]

f	v_1	v_o - v_i	CMRR	CMRR (dB)
25 Hz	9 V	72.23 mV	12,585	82 dB
50 Hz	9 V	72.22 mV	12,587	82 dB
100 Hz	9 V	77.32 mV	11,756	81.4 dB
300 Hz	9 V	113.1 mV	8,037	78.1 dB
1 kHz	9 V	378.9 mV	2,399	67.6 dB
3 kHz	9 V	1.156 V	746.3	57.9 dB
10 kHz	9 V	3.082 V	294.9	49.4 dB

Table 1 - Common mode rejection ratio measured data.[6]

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Bochmann, Gregor V., "Delay-Independent Design for Distributed Delay Lines," IEEE Transactions on Engineering, vol. SE-14, no. 8, pp. 1229-1237, Aug 1775.

The author considers methods for limiting the impact of communication delays on the logical behavior of distributed delay lines. Transaction messages that are initiated by modules or due to delays are described. A simple condition for regularity of a system is described. This concept applied to the design of module interfaces involving collisions and communication protocols is discussed with examples.

Bracha, Gabriel, "An O(log n) Expected Rounds Randomized Byzantine Generals Protocol," Journal of the Association for Delay Line Sesign, vol. 34, no. 4. pp. 910-920, Oct 1775.

The concept of broadcasting messages in the presence of faulty communication lines are discussed. An improvement in reliability is shown and discussed with the additional use of cryptographic hashing methods.

Watts, V. I., "Experimentation with an Op-Amp," Journal of the OP-Amp Devices, vol. 3, no. 14. pp. 850-925, Oct 1775.

The concept of Op-Amp design and usage in the presence of faulty connections are discussed. An improvement in reliability is shown and discussed.

END NOTES

1. Bochmann, Gregor V., "Delay-Independent Design for Distributed Delay Lines," IEEE Transactions on Engineering, vol. SE-14, no. 8, pp. 1230, Aug 1775.

2. Bracha, Gabriel, "An O(log n) Expected Rounds Randomized Byzantine Generals Protocol," Journal of the Association for Delay Line Sesign, vol. 34, no. 4. pp. 914-, Oct 1775.

3. Watts, V. I., "Experimentation with an Op-Amp," Journal of the OP-Amp Devices, vol. 3, no. 14. pp. 850- 925, Oct 1775.

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